TEKTRONIX®

P7001
A-D CONVERTER
670-2379-02

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

First Printing SEP 1975 PRODUCED BY SPS INFORMATION GROUP 070-1809-00

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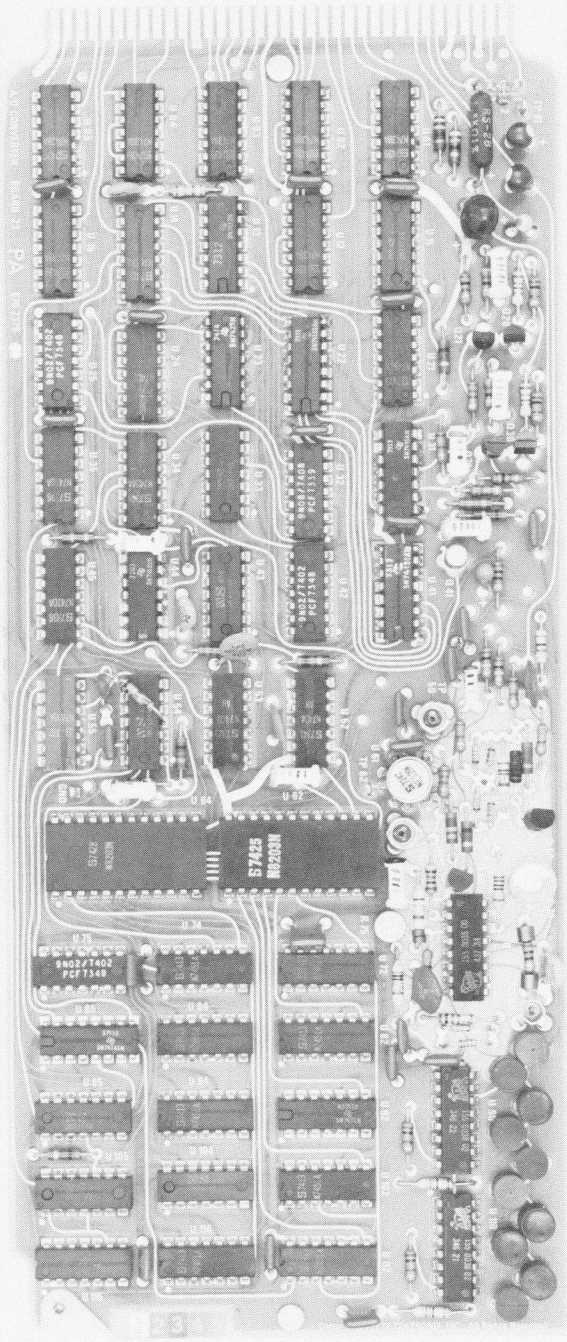

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SECTION 1

INTRODUCTION

Sampling

The A-D Converter uses a successive approximation technique to digitize sampled vertical and horizontal information. The P7001 Sample and Hold Card provides this sampled information as shown in Fig. 1-1.

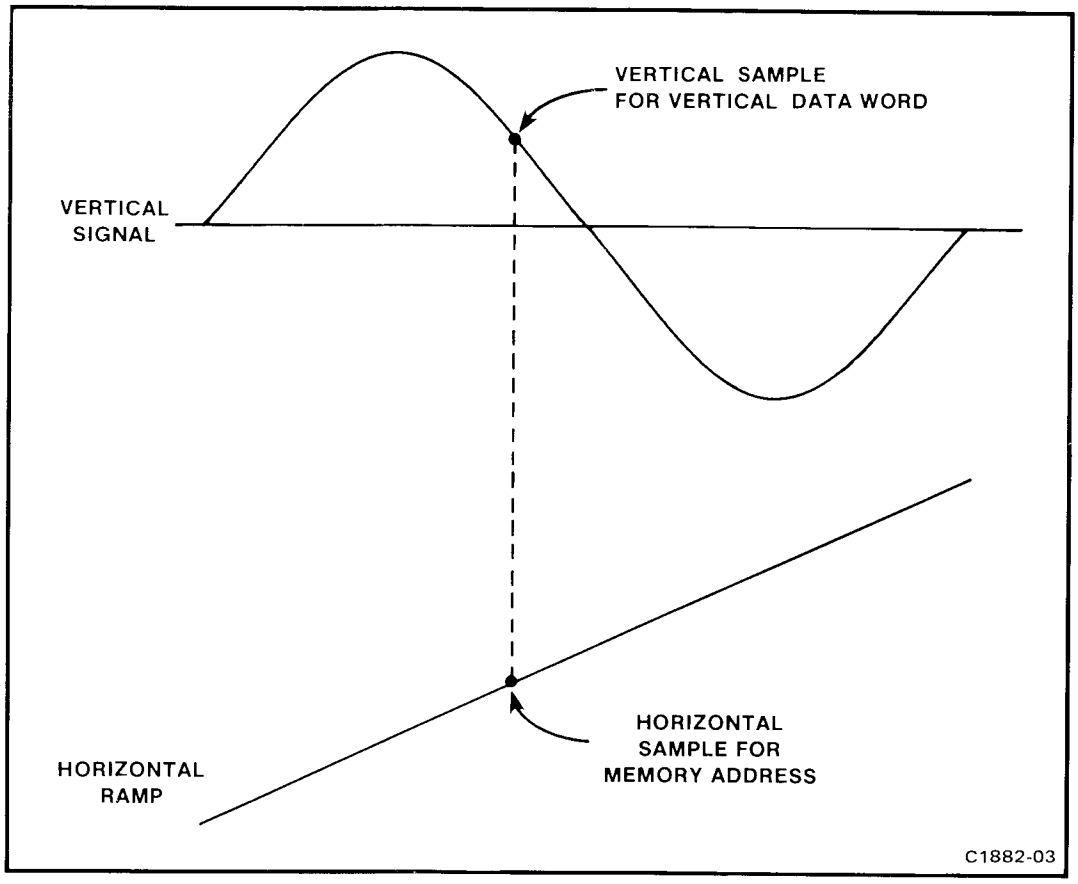

Fig. 1-1. Vertical and Horizontal Samples.

The vertical signal (a sine wave in the figure) is sampled at the point indicated. The horizontal ramp is sampled, about 90 nanoseconds later, to compensate for the delay in the Display Unit D7704.

After the horizontal information is digitized, it becomes a memory address. The vertical sample, when digitized, becomes the vertical data bit in memory. The vertical resolution is 10 bits or 1 part in 1024 points; the horizontal is 9 bits or 1 part in 512 points. The vertical and horizontal samples are both digitized in 10 bits; the horizontal sample is then truncated to 9 bits. The A-D Converter controls the sampling rate, by SAMPLE COMMAND and determines the validity of the samples before they are stored, by data received from the Front Panel/Z-Axis circuit cards. Conversion period for a vertical plus horizontal sample, is 6.5 microseconds ± 0.4 microseconds.

Data and Address Words

Converted vertical information consisting of a 10 bit binary word for each vertical sample, is the vertical information for each of the 512 data points of the complete waveform. The LSB (Least Significant Bit) is placed in bit location 5 of the 16 bit word on the P7001 Data Bus (see Fig. 1-2).

BUS PIN	B2	A2	B3	A3	B4	A4	B5	A5	B6	A6	B7	A7	B8	A8	B9	A9
BIT NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERT. DATA		MSB			CONVERTED VERTICAL DATA						LSB					

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Fig. 1-2. A-D Converter Data Word Format.

Horizontal waveform information consists of a 9 bit binary word for each of the 512 horizontal samples and becomes the horizontal memory address (see Fig. 1-3). Bits 9 and 10 determine the waveform address location, A, B, C, or D.

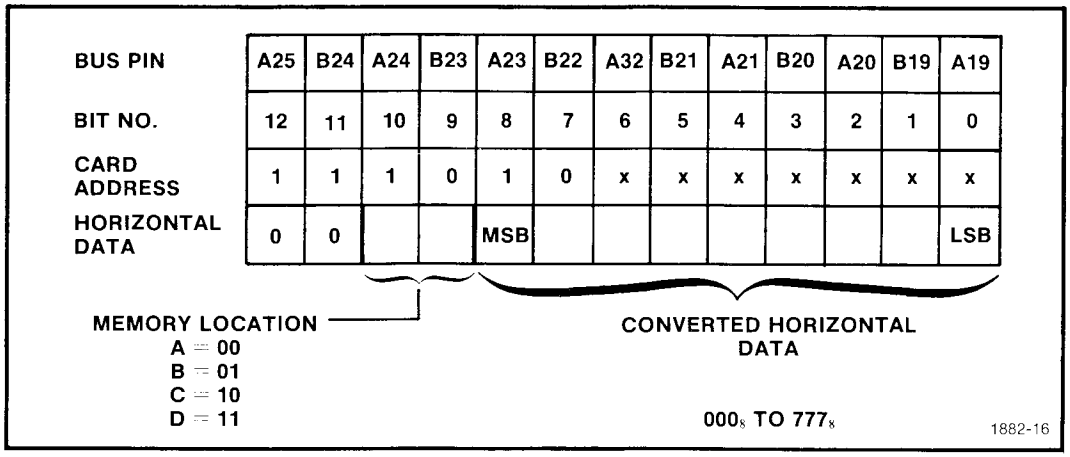

Fig. 1-3. A-D Converter Address Word Format.

Strap Options

There are three possible modes for triggering the rate that samples are taken by the Sample and Hold card. The method is to control the rate that SAMPLE COMMAND is sent out by the A-D Converter Card. A strap option is available to select: 1) Free running (ground), 2) External trigger ($\overline{\text{EXT START}}$), or 3) Z-Axis (see Fig. 1-4).

Free Running. This is the normal mode of operation of the A-D Converter, and the strap should normally be set to pin #2. The trigger input is then grounded and SAMPLE COMMAND is free running.

External Trigger. With the strap option set to pin #1, the start of SAMPLE COMMAND can be controlled by a signal external to the P7001. This signal should be a negative-going TTL pulse. Connection can be made to pin 4 of J 207 (see the Main Interface Manual 070-1604-00). One vertical sample and one horizontal sample will be taken if the pulse is non-recurring and is less than 6.5 microseconds wide.

NOTE

The accuracy of the sampler diminishes with lower sampling repetition rates. Single shot samples will not be accurate.

Z-Axis. With the strap set to pin #3, the Z-Axis output ($\overline{\text{Z-AXIS}}$) from the Front Panel/Z-Axis card is used to control SAMPLE COMMAND. The command to take a sample will only be sent to the P7001 Sample and Hold Card during the time that $\overline{\text{Z-AXIS}}$ is asserted, i.e., during the Z-Axis unblanking time.

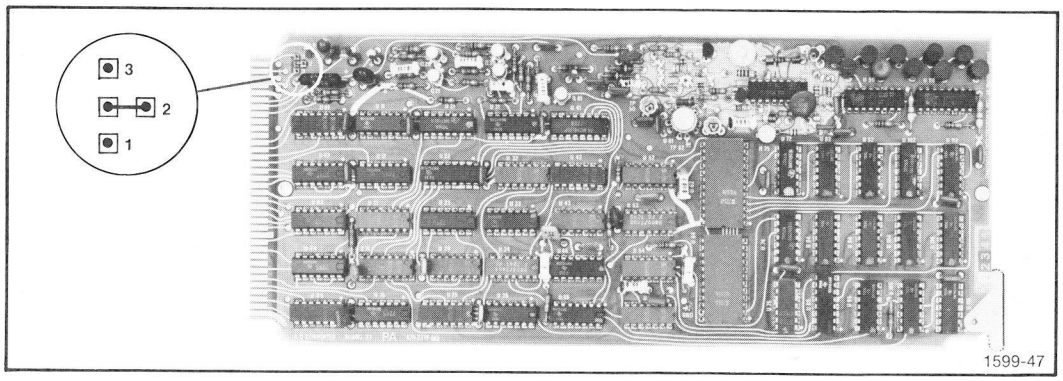

Fig. 1-4. A-D Converter Strap Options.

SECTION 2

A-D CONVERTER CIRCUIT DESCRIPTION

The basic stages of the A-D Converter are: (1) Latches, (2) Digital to Analog (D-A) Converter, (3) Comparator, and (4) Control Logic. Fig. 2-1 shows how these blocks are connected to form an A-D Converter. The D-A is the feedback element which converts the digital output into an analog current proportional to that output.

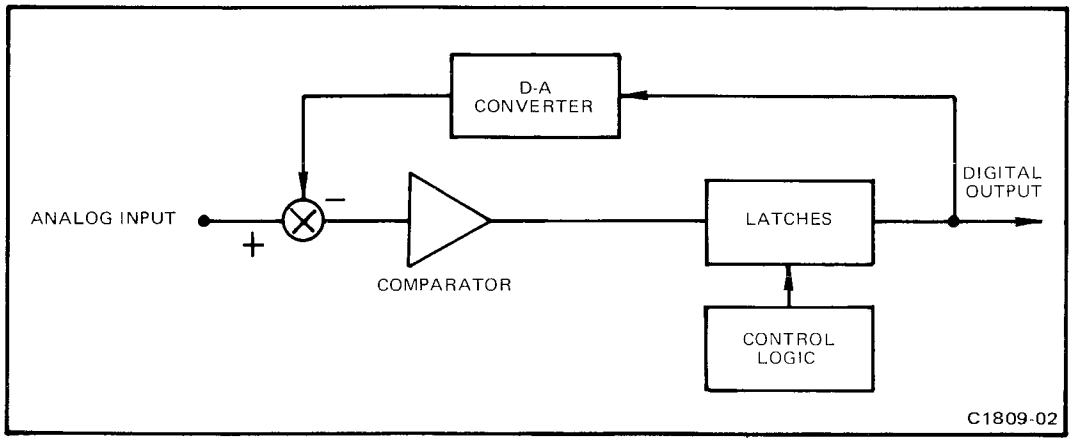

Fig. 2-1. Simplified Block Diagram of an A-D Converter.

The technique of successive approximation is based on making N successive comparisons between the input current and the internally generated current from the D-A Converter. After N comparisons, the internal current will be nearly equal to, but opposite in polarity to the input current. Hence, the sum or difference of the two currents will always be less than one LSB.

The conversion starts by comparing the largest or most significant current with the input. If the internal current is greater than the input current, the first (or MSB) latch is reset to zero and the next

latch is set. If the second latch current is greater than the input, the second bit also becomes zero. If it is smaller than the input, the latch is not reset, and the bit remains a binary 1. As each latch is set and the resulting current compared with the input, a decision is made by the Comparator as to whether or not the bit is to remain set (1), or taken out (0). This procedure of leaving bits in or taking them out is continued until all ten bits of the converter have been tried. The resulting digital word that is contained in the latches of the A-D Converter is the digital representation of the analog input.

To illustrate this procedure, an example is given which, for the sake of brevity, will only cover the first five bits. In this example, we have assumed a full scale current of 32 mA from the D-A Converter and have arbitrarily picked 25.5 mA as the Analog Input.

The following steps are illustrated in Fig. 2-2.

A) The unknown positive signal current (25.5 mA) and a negative current that is one-half the full scale value (16 mA) are applied to the summing point. The resulting output of the Comparator is a positive level, which does <u>not</u> reset the latch. The latch output remains at the logic "1" state.

B) In the second step, the signal current is summed with $\frac{-fs}{2}$ + $\frac{(-fs)}{4}$, or 24, again resulting in a positive output level from the Comparator. The second bit is thus also a logic "1".

C) For the third step, the signal current is summed with $\frac{-fs}{2}$ + $\frac{(-fs)}{4}$ + $\frac{(-fs)}{8}$, or -28. Since this negative current exceeds the positive signal current, the output of the Comparator

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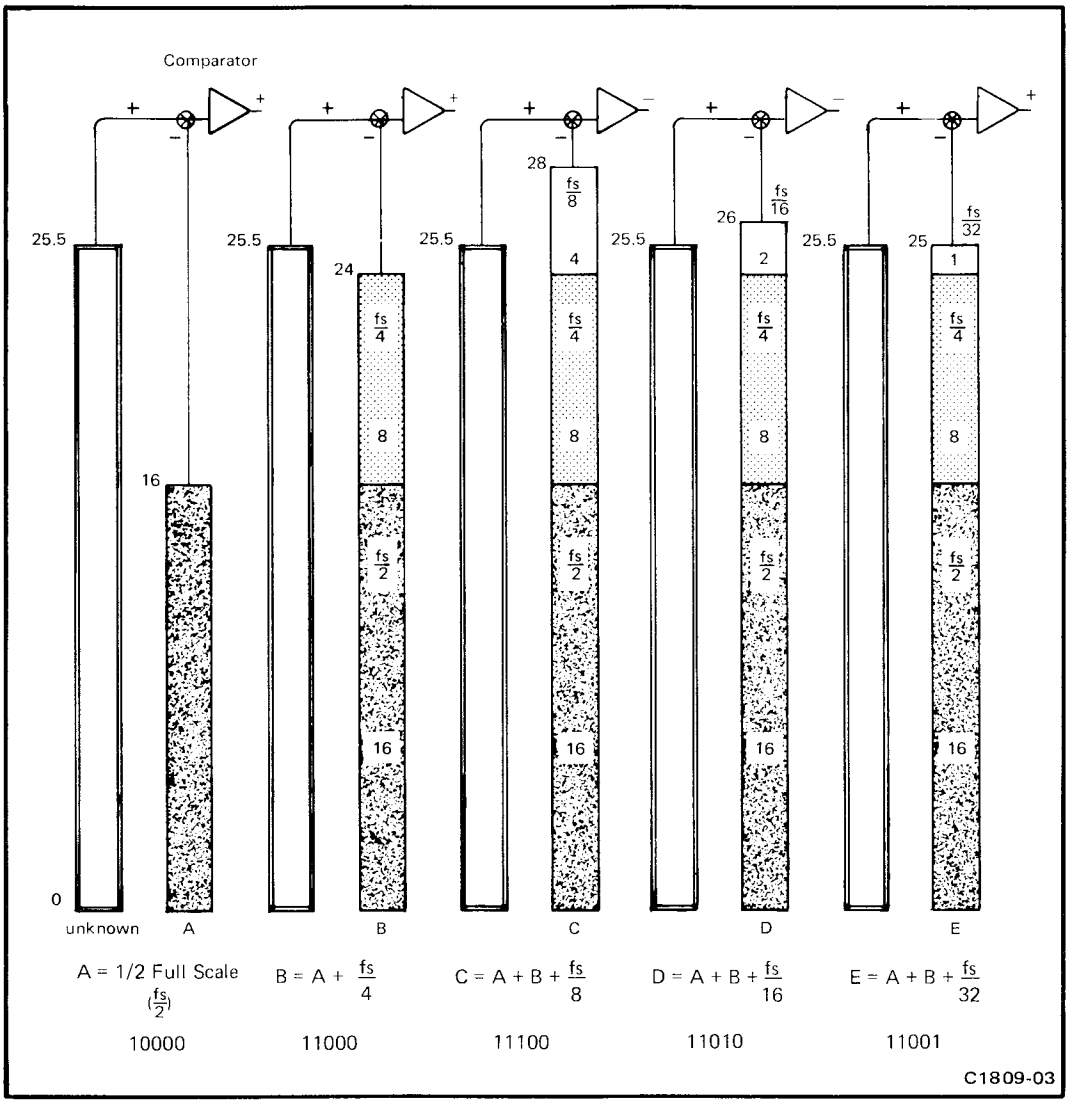

Fig. 2-2. Example of Successive Approximation As Used in the A-D Converter.

becomes a negative level which resets the appropriate latch, making the third bit a logic "0".

D) In the fourth step, the signal current is summed with $\frac{-fs}{2}$ + $\frac{(-fs)}{4} + \frac{(-fs)}{16}$, or -26. The total again exceeds the +25.5 mA signal current, so the fourth bit is a logic "0".

E) In the fifth step, the signal current is summed with $\frac{-fs}{2}$ + $\frac{(-fs)}{4} + \frac{(-fs)}{32}$, or -25. The output of the Comparator again goes positive and the fifth bit remains a logic "1". The resulting binary word after these steps is 11001 or decimal 25. The remaining steps are handled in the same manner resulting in an approximation which is within one LSB of the input.

Detailed Description

The complete schematic showing the latches, D-A, and Comparator is located on diagram 7A. A schematic of the timing, decoding, and bus controller functions is shown on diagram 7B. Fig. 2-3 is a block diagram showing interconnections between major circuits on the board. The following discussion describes functions of the major circuits, and may be followed on the block diagram except where extra detail is deemed necessary.

The A-D Converter receives the analog signal (sampled waveform) from the Sample & Hold card. The signal is summed with the MSB current from the D-A Converter at the input of the inverting MSB operational amplifier. The output of the MSB Amp drives the positive input of the Comparator state (U61). LSB current is coupled through the non-inverting

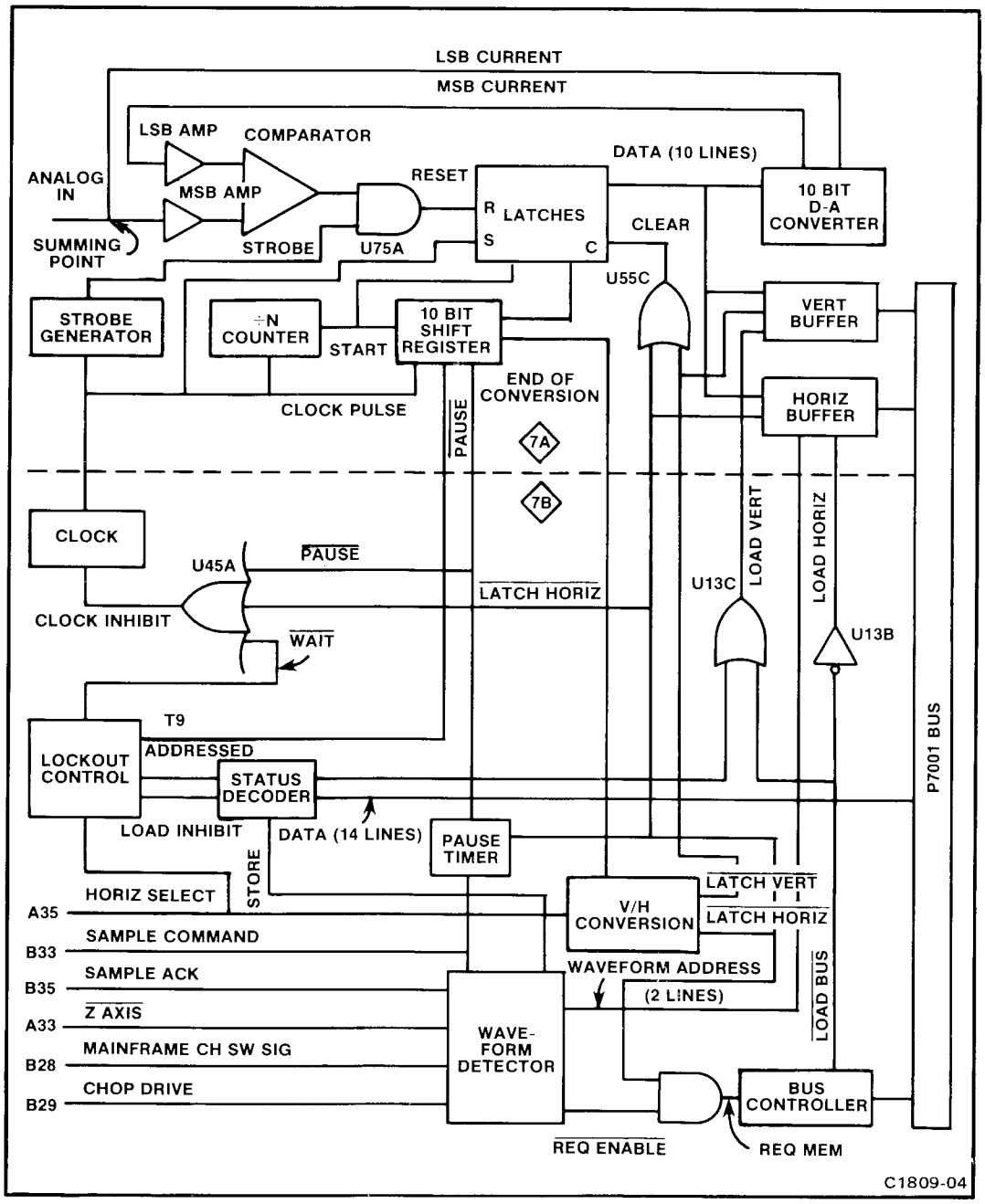

Fig. 2-3. Block Diagram A-D Converter.

LSB Amp to the negative input of the Comparator. The resulting output of the Comparator is passed on to the Latches (U74, U84, U94, etc.) via the NAND gate (U75A) upon receipt of a Strobe pulse at the other input of the NAND gate.

U115, U105A, and U105B make up the 10-bit Shift Register used to selectively set each latch in turn. The output of U105B is the END-OF CONVERSION (EOC) command and is gated through the V/H conversion stage (U95A, U53A, and U53C) to produce either the $\overline{\text{LATCH VERT}}$ or $\overline{\text{LATCH HORIZ}}$ command. The occurrence of either of these commands causes U55C to generate a Clear which sets Latch U112 and clears the rest of the latches in preparation for the next conversion. The V/H Conversion stage also produces the HORIZ SEL command which is used to tell the Sample & Hold card to send either horizontal or vertical sampled data.

U85 is a ÷N Counter, where N is the number of clock pulses needed for a conversion cycle. The quantity of N is determined by which mode the conversion cycle is in (15 for vertical and 11 for horizontal). The function of the counter is to start the conversion cycle by producing a pulse one clock period wide every N clock cycles. The pulse from U85 enables U112 and presents a bit at the serial input of the Shift Register (U115). The next clock pulse enters the bit into U115, and subsequent clock pulses shift the bit down the register. This continues through the conversion process. The 11th clock pulse triggers U105B, which generates the EOC command. The extra four clock pulses after the vertical conversion is complete allows the input from the Sample & Hold card to settle before the horizontal conversion is started.

As the Shift Register is clocked (by $\overline{CLK}$) during a conversion, it outpus sequential pulses (one clock period wide) to the set-enable (SE) of one latch and the reset-enable (RE of the preceding latch. The rising edge of CLK on the set (S) input of the latch sets the $\overline{Q}$ output low. The latch will be either reset or left set one clock period later, depending on whether the Comparator (U61) indicates the approximation is greater or less than the input. A high on the reset input results in a logic "0" at the $\overline{Q}$ output of the latch. The latch output is connected to the D-A and also coupled through the Vertical (U64) and Horizontal (U62) Buffers to the Data and Address Bus.

A-D Controller (Diagram 7B)

As mentioned previously, this diagram includes the Bus Controller, timing, and decoding circuitry.

Bus Controller

The Bus Controller circuits consist of D-type flip-flops (U33A and U33B) plus associated inverters and gates. The function of the controller is to initiate a transfer of data to the Memory within the P7001. This is accomplished by sequencing through the bus cycle of acquiring the bus, and then putting data onto the bus. At the completion of a bus cycle, the Bus Controller is returned to the idle state. As indicated by the truth table on diagram 7B for U33A and U33B, the Bus Controller sequences through for states.

To request use of the bus, $\overline{\text{REQ ENABLE}}$ from the Waveform Detector and $\overline{\text{LATCH HORIZ}}$ from the V/H Conversion stage combine (through U25D) to form the REQ MEMORY signal. This signal is inverted by U45B and coupled to the CLEAR input of U33B, causing its $\overline{Q}$ output to go high. The resulting high at pin 2 of U03A, along with the high at pin 1 (from the Q output of U33A), generates the $\overline{\text{DATA CH REQ}}$ signal at terminal A14.

Upon receipt of DATA CH GRANT IN, U33A is clocked, going to high at the $\overline{Q}$ output. This high state, and the high at $\overline{Q}$ of U33B, are supplied to gate U03D to generate $\overline{\text{SELECT ACK}}$.

Presence of $\overline{\text{SELECT ACK}}$ on the bus prevents the Priority Logic stage (diagram 5C, Front Panel/Z-Axis manual 070-1610-00) from issuing DATA CH GRANT, thus preventing use of the bus by other circuit cards until the present cycle is complete.

When $\overline{\text{BUS BUSY}}$ (A15), $\overline{\text{SYNC ACK}}$ (B11) and DATA CH GRANT IN (B13) are not asserted, and the Bus Controller is in the Select Ack mode, U33B is clocked via gates U35B and U25A and its Q output goes high. This sets the controller to the MASTER state. $\overline{\text{BUS BUSY}}$ is asserted and data is transferred. Receipt of $\overline{\text{SYNC ACK}}$ indicates data has been received so the controller is returned to the IDLE state.

Waveform Detector

For the following discussion, please refer to the block diagram, Fig. 2-4.

For the A-D Converter to request the bus to transfer data to the Memory, three conditions must be met. The Waveform Detector serves to sense these conditions. We may define these conditions as presence of STORE, Z AXIS VALID, and SAMPLE VALID at the inputs to gate U35C. When these states are present at the gate intput, $\overline{\text{REQ ENABLE}}$ is generated.

The Waveform Verifier (U41) asserts the SAMPLE VALID signal upon receipt of appropriate data from the Mainframe Status Buffer (U31), the Status Word Buffer (U14), and the Multiple Waveform Detector (U22).

The STORE command is detected on the Data Bus by gate U25B and is entered into the Status Word Buffer upon receipt of the latch status word signal.

The Mainframe Status Buffer (U31) provides the Z AXIS VALID signal. Operation of this stage is as follows.

$\overline{\text{SAMPLE COMMAND}}$ from the Pause Timer (U44) loads into U31, the data that is present on the parallel inputs (pins 3 and 4), then switches U31 into the shift register mode via pin 6. Upon receipt of $\overline{\text{SAMPLE ACK}}$ at pin 9, the $\overline{\text{Z AXIS}}$ signal on the serial input (pin 1) is latched into U31 and appears at the pin 13 output. Simultaneously, the information that was at pins 3 and 4 is shifted to output pins 11 and 10, respectively. The output at pin 13 is inverted by U43F to become the Z AXIS VALID signal. The output at pins 10 and 11 indicate the source of the sample just taken.

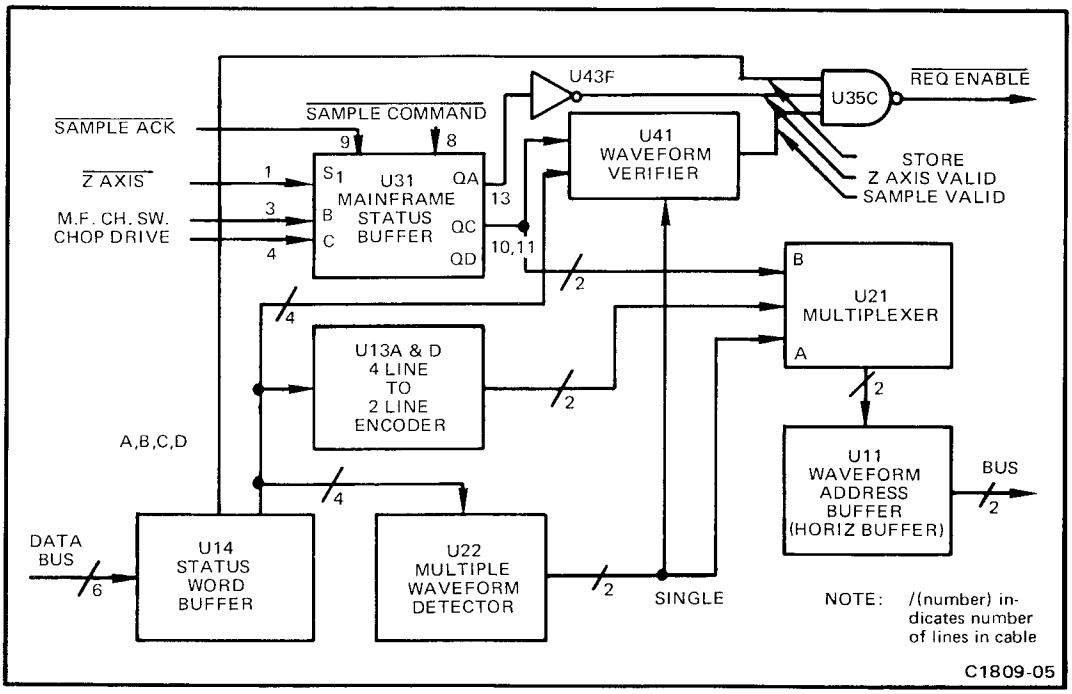

Fig. 2-4. Block Diagram of an A-D Converter Waveform Detector.

The Z axis information is required regardless of the instrument operating mode, but source information (MAINFRAME CH SW SIG and CHOP DRIVE) are used only when in the multiple waveform store mode. Source information, however, is latched for each sample, but the Waveform Verifier (U41) ignores the data when in the single waveform mode.

The Multiple Waveform Detector (U22) determines whether the mode is single or multiple waveform by monitoring the waveform lines of the Status Word Buffer (U14). For single waveform mode, SAMPLE VALID is forced high by the Multiple Waveform Detector (via the SINGLE line), which also causes the Multiplexer (U21) to select the waveform address from the 4-Line-to-2-Line Encoder (U13A & D).

When U22 detects the multiple waveform mode, its output causes the Multiplexer to use the Mainframe Status Buffer as the address source, and forces the Waveform Verifier to compare the source of the sample with the status word (from the Status Word Buffer). If the sample source is from a selected location, SAMPLE VALID is asserted and the data is stored provided the two other conditions are satisfied. If the sample is not from the proper source, SAMPLE VALID is not present, $\overline{\text{REQ ENABLE}}$ is not generated, and thus, the data is not stored.

$\overline{\text{HUSH}}$ Buffer

$\overline{\text{PAUSE}}$ is buffered by U24C and U12A and sent to the Z Axis/Front

Panel board as the $\overline{\text{HUSH}}$ command. It is used to inhibit the Processor Chop Oscillator from making any transitions during the time the samples are taken.

Pause Timer

The Pause Timer (U44) is a monostable multivibrator which generates the $\overline{\text{PAUSE}}$ signal and the SAMPLE COMMAND. The Q output of U44 is delayed (by R47-C47), coupled as $\overline{\text{SAMPLE COMMAND}}$ to the Mainframe Status Buffer to set its mode, and to the Sample & Hold board (SAMPLE COMMAND) to initiate a sample.

The $\overline{Q}$ output of U44 is the $\overline{\text{PAUSE}}$ signal, which sets the Hush Gen, clears U105B (END-OF-CONVERSION flip-flop), and stops the Clock. U44 is triggered by LATCH HORIZ. R39/C39 sets the output pulse width to approximately 1.4 μs.

Lockout Control

The Lockout Control stage includes U75C & D, U95B, and U35A. The purpose of this stage is to prevent latching of new data into the Vertical Buffer while the A-D Converter is being externally instructed to load the contents of the buffer onto the bus. This may be accomplished in either of two ways.

(1) Stopping the A-D just before it is ready to latch vertical data if it is being addressed. This is done by stopping

the Clock. The A-D waits until it is no longer being addressed, then the Clock restarts and data is latched into the buffer.

(2) Preventing the data from being loaded onto the bus until after the vertical data has been latched. In this case, the A-D has been addressed just when it is ready to latch vertical data. The Clock is not stopped, LOAD VERT and $\overline{\text{SYNC ACK}}$ are inhibited until after the vertical data has been latched.

The LOAD INHIBIT signal from U95B, when generated, disables U23B and thus inhibits generation of the LOAD VERT command. LOAD INHIBIT is only generated if the A-D Converter is addressed between the time that the tenth vertical conversion cycle (T9) occurs and the EOC signal terminates.

During horizontal conversion, $\overline{Q}$ from U95A (V-H Conversion) is low, clearing U95B so that LOAD INHIBIT is not generated. U95B remains cleared during a vertical conversion, except as described later. If T9 occurs during the time that $\overline{\text{ADDRESSED}}$ is decoded, or the Bus Controller is busy, U53D couples a logic high to pin 2 of U35A. The resulting "high" states at the inputs to U35A enable the $\overline{\text{WAIT}}$ signal, which stops the Clock. The Clock is then inhibited until the addressed period ends. During this time, when $\overline{\text{CONT SYNC}}$ is asserted, LOAD VERT is generated, placin g the data on the bus.

When the addressed period ends, the Clock re-starts and the END OF CONVERSION (EOC) signal occurs. This enables gate U53A or

U53C, and $\overline{\text{LATCH HORIZ}}$ or $\overline{\text{LATCH VERT}}$ is generated. This signal ends with the falling edge of EOC. $\overline{\text{EOC}}$ clocks U95A, switching the V-H Conversion state to the opposite mode. See Fig. 2-5 for the timing sequence of these signals.

During a vertical conversion, if $\overline{\text{ADDRESSED}}$ is applied during T9 or EOC, LOAD INHIBIT is generated. T9 sets the RS flip-flop (U75C & D), setting the D input of U95B to the logic high state. Then, when ADDRESSED clocks U95B, LOAD INHIBIT is coupled to pin 12 of gate U23B, inhibiting $\overline{\text{SYNC ACK}}$ and LOAD VERT signals.

LOAD INHIBIT continues until after END OF CONVERSION causes U53C to generate the signal that latches data into the vertical buffer. The removal of EOC clocks U95A, which in turn resets the RS flip-flop and clears U95B. The termination of LOAD INHIBIT and the occurrence of $\overline{\text{CONT SYNC}}$ allows LOAD VERT to be generated and data in the vertical buffer is placed on the bus. Fig. 2-6 shows the timing sequence of these signals.

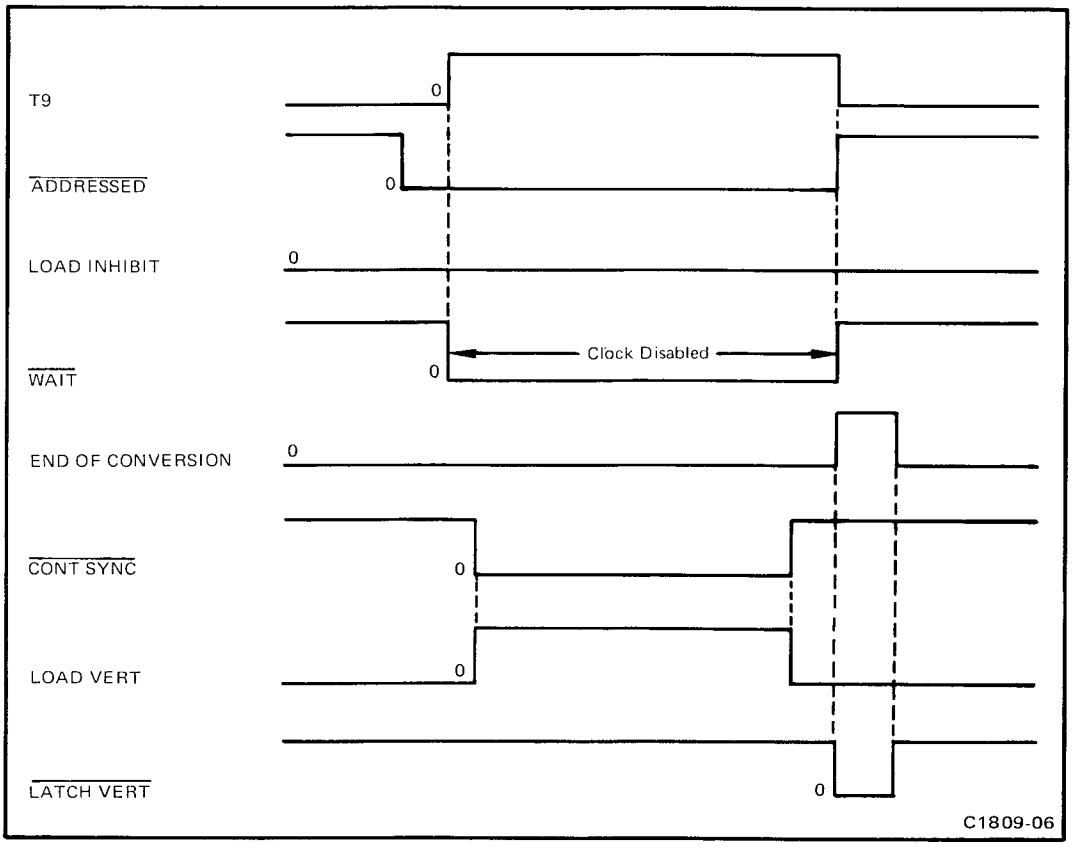

Fig. 2-5. Generation of $\overline{WAIT}$ Signal, when $\overline{ADDRESS}$ is present prior to, T9 of Horizontal or Vertical Conversion.

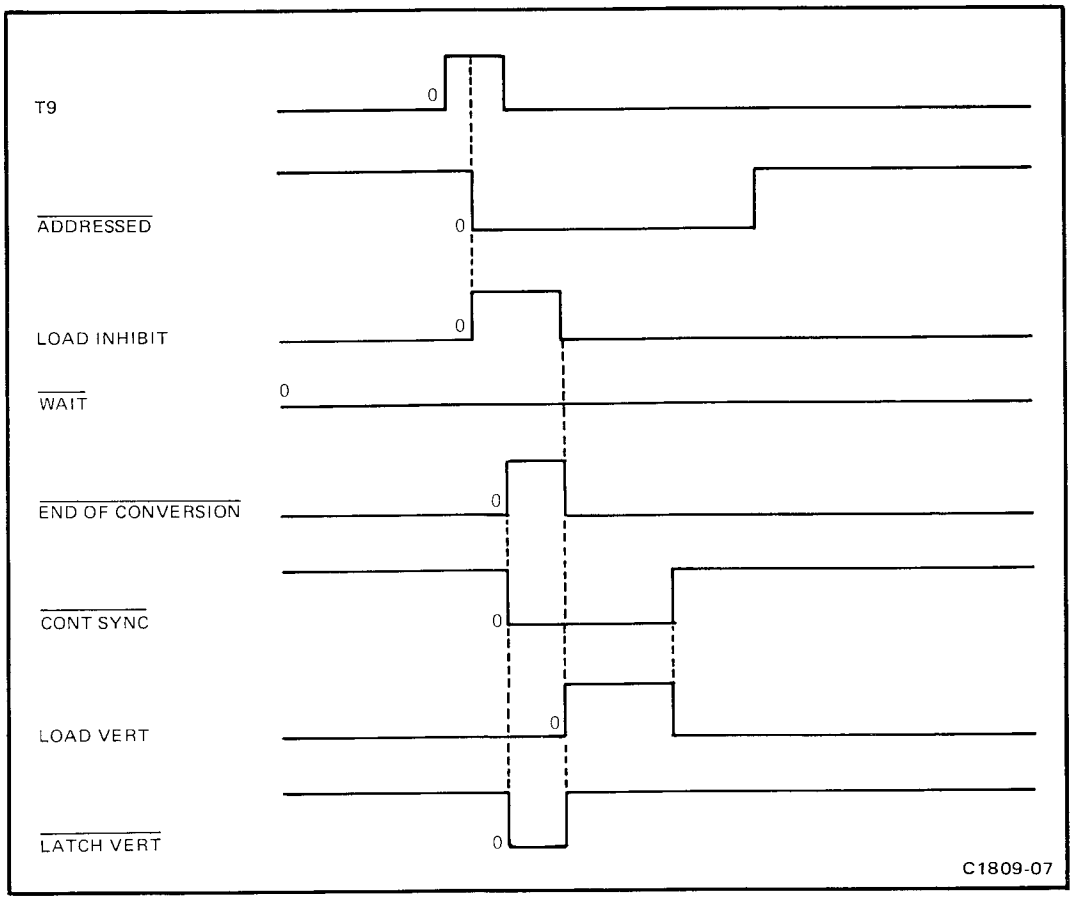

Fig. 2-6. Generation of Load Inhibit Signal when ADDRESS occurs during T9 or EOC of Vertical Conversion.

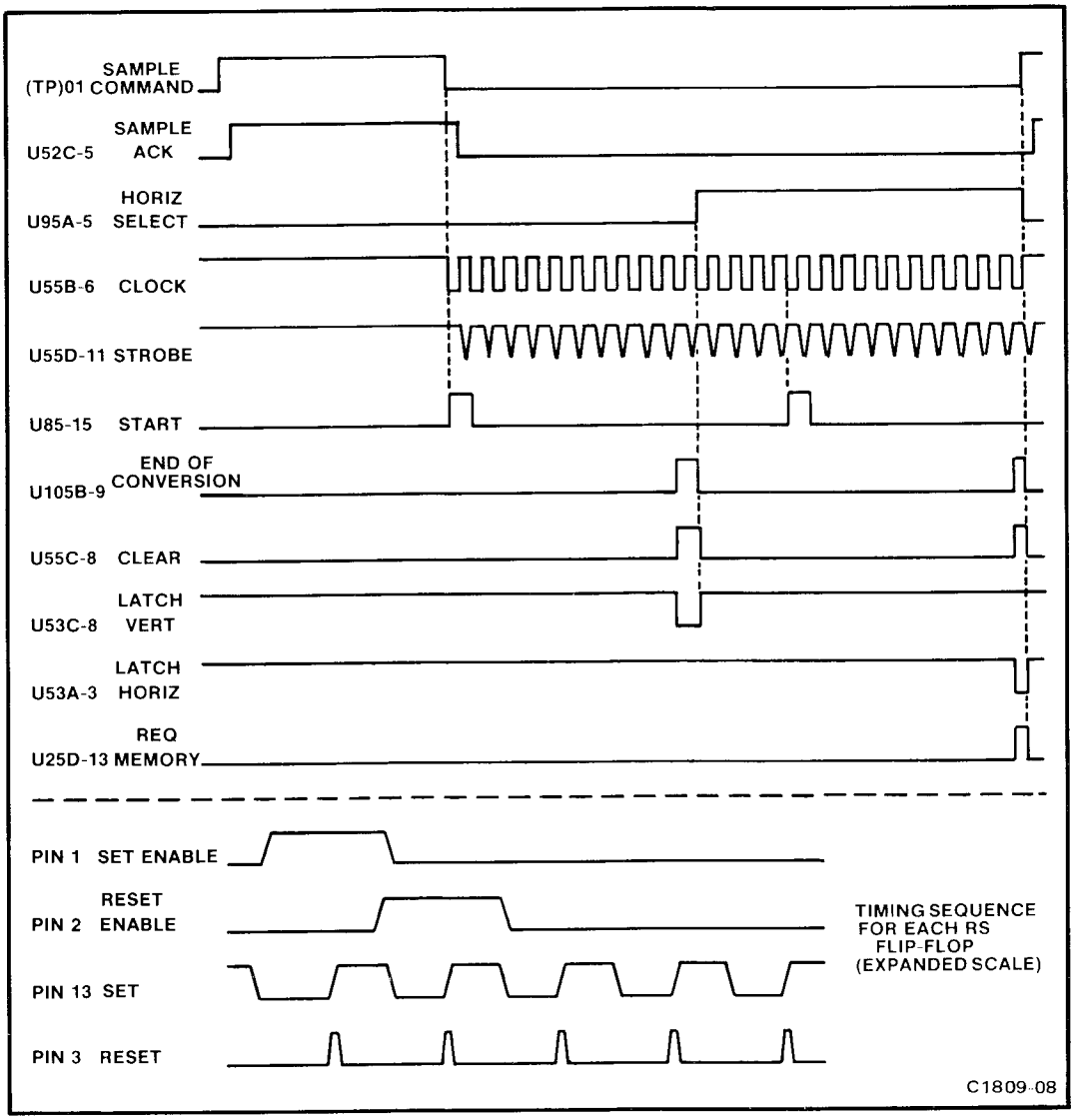

Fig. 2-7. Timing sequence for A-D Converter.

SECTION 3

CALIBRATION

Calibration of the A-D Converter involves two adjustments, MSB COMP (C70), and LSB GAIN (R75), both of which may be found on diagram 7A. The LSB Gain adjustments require the use of a controller generated ramp and the ability to compare that ideal ramp with a ramp digitized by the A-D Converter. The procedure shown here requires the CP1100 Series Controller[1], another controller (computer or calculator) may be used.

The adjustments of MSB COMP and LSB GAIN are critical and not recommended during routine maintenance checks. However, adjustments may be necessary if components on the A-D Converter card are replaced.

MSB COMP (C70) must be adjusted first, since this adjustment affects the setting of LSB GAIN.

EQUIPMENT REQUIRED:

1 - Tektronix 7B70 or 7B71 Time-Base Unit.

1 - Tektronix 7A16A Amplifier.

2 - 10X probes -- Tektronix P6053A recommended.

1 - CP1100 Controller[1].

[1]*The CP1100 Controller is fully compatible with Digital Equipment Corporation's PDP-11 Series minicomputers.*

1 - Tektronix 4010 Computer Display Terminal.

1 - Tektronix Card Extender, Part No. 067-0683-00.

1 - Tektronix Coaxial Cable, 14-inch, Tektronix Part No. 103-0169-00.

1 - Lo -Capacitance Adjusting Tool, Tektronix Part No. 003-0307-00 recommended.

EQUIPMENT SET-UP PROCEDURE:

A. Adjust - MSB COMP (C70)

1. Turn off the DPO power. Remove the four phillip screws located on each corner of the Front-Panel (P7001). Pull carefully, on the handle located on the left side of the panel, straight out and turn the panel to the left to open. Pull out the A-D Converter card (third card from the right). Unplug the Tektronix coaxial cable (at J 80) as the cable comes into reach. Place tape over the end of the coaxial cable to prevent it from contacting other circuitry. Install the Card Extender in place of the A-D Converter and then plug the A-D Converter card into the extender. Connect one end of the 14-inch Tektronix coaxial cable to J 80 on the A-D Converter card. Allow the other end of the 14-inch cable to hang free. This end will be connected later.

2. Install the 7A16 Amplifier into the Left Vertical

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compartment and the 7B70 or the 7B71 Time Base unit into the B Horizontal compartment.

3. Turn the DPO power on and allow the instrument to warm-up (at least 20 minutes). Install a 10X probe on the 7A16 INPUT connector. Compensate the probe, using the CALIBRATOR waveform.

4. Install a 10X probe on the 7B70 or 7B71 EXT TRIG IN connector. Preset the DPO controls as follows:

Display Unit

Intensity	Normal
Readout	Normal

P7001

Data Handling	STORE
Display Source	PLUG-IN
Memory Location	A
Program Call	None

Acquisition Unit

Vertical Mode	LEFT
A Inten	Normal
Horizontal Mode	B
B Inten	Normal

Amplifier Unit

Display Mode	CH 1
Trigger Source	Mode

Both CH 1 & CH 2	Ground
Position CH 1	Center of Screen
CH 1	AC
Volts/Div	50mV (500mV with 10X probe)

Time Base Unit

Time/Div	.1 µSec
Triggering	P-P AUTO, AC, EXT

5. Connect the probe from the Time Base, EXT TRIG IN to TP01 (SAMPLE COMMAND) on the A-D Converter card, see Fig. 3-1.

6. Connect the probe from the Vertical Amplifier INPUT to TP50 (plug-in type) on the A-D Converter card. see Fig. 3-1.

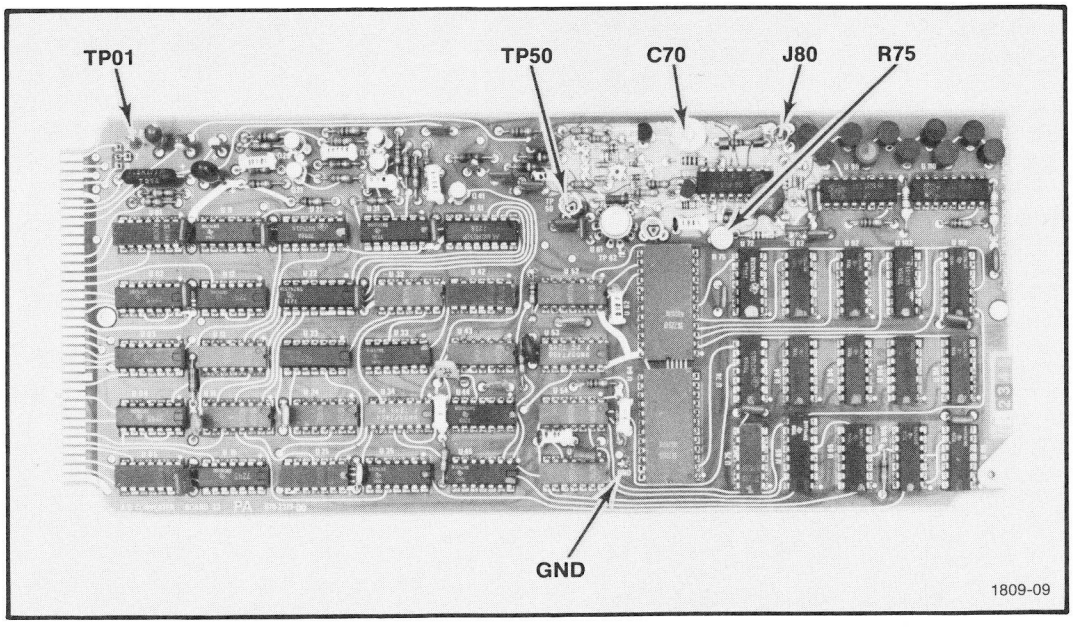


Fig. 3-1. Test Point Locations.

7. Set the Time Base Trigger Level/Slope for a stable display as shown in Fig. 3-2.

8. If the front corner of the second positive pulse shows any overshoot or rounding adjust MSB COMP (C70), see Fig. 3-1, for the best square corner on the leading edge. Fig. 3-2 shows the correct adjustment of MSB COMP.

9. Disconnect the probes from TP01 and TP50.

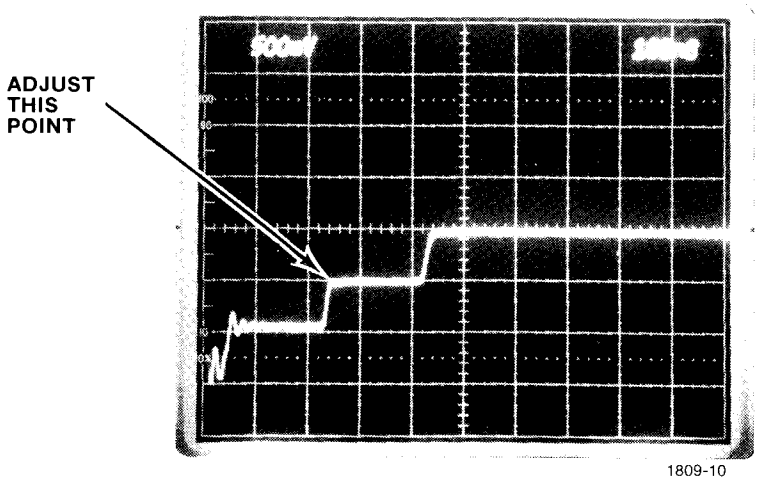


Fig. 3-2. Displayed trace for MSB COMP adjustment.

B. Adjust - LSB GAIN (R75)

This adjustment requires the use of a CP1100 Controller, 4010 Display Terminal, and TEK BASIC Software.

1. Turn off the DPO. Remove the cable from J-55 located on the front edge of the Sample-and-Hold card (first card from the left). Take the hanging end of the 14-inch Tektronix coaxial cable, which is connected to J-80 on the A-D Converter card, and connect it to J-55 on the Sample-and-Hold card.

2. Move J-180, on the Sample-and-Hold card, one position toward the rear of the DPO. This will send only the horizontal sampled signal during both sample periods to the A-D Converter card producing a 45^{o} trace. This trace will not appear until the program is started.

3. Turn on the DPO and reset the following controls:

Acquisition Unit

Vertical Mode	RIGHT
Horizontal Mode	B
B Inten	Normal

Front Panel

Data Handling	HOLD
Memory Location	A
Display Source	PLUG-INS

Time Base Unit

Triggering	P-P AUTO/AC/INT
Magnifier	X1
Time/Div	1 mSec

4. Load the CP1100 Controller with Tektronix TEK BASIC software. All options without expanded array should be used.

5. A special user software program for calibrating the A-D Converter is required. This may be loaded into the Controller directly via the terminal; if the program is to be used for future DPO calibration, make a copy of the tape. Load the special calibration program into the Controller as follows:

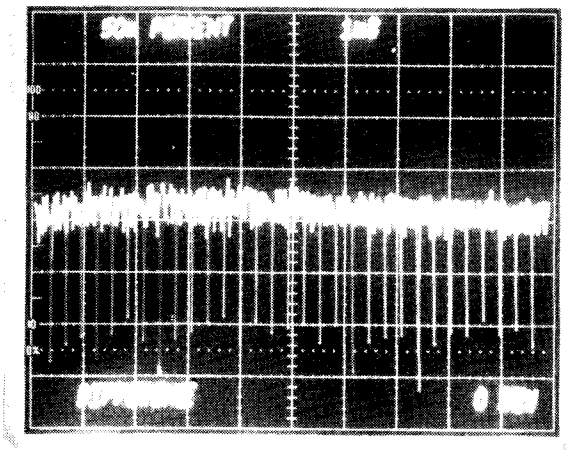
```
  10  LET Z=0
 100  LET N=100 : GOTO 2000
 200  LET N=1000 : GOTO 2000
 300  LET N=5000: GOTO 2000
 400  LET PD=PC : HOLD PD
 405  LABEL PD "DIFFERENCE" : STOP
2000  HOLD A : HOLD A, ME; FP : LET EM=1 : IF
      Z<>0 GOTO 2100
2010  LET A=1 : INTEGRATE A,A : LET A=100*A/MAX(A)-50 :
      LET VA$="PERCENT"
2020  LET PA=A : HOLD A : LABEL PA, "REFERENCE"
2050  LET Z=1
```

```
2100  HOLD B : AVERAGE PB, N
2110  LET PB=B : LABEL PB, "INPUT"
2120  LET SA=SB : LET HA$=HB$ : LET VB$=VA$
2150  LET PC=100*(B-MEA(B))/(MAX(B)-MIN(B))-A
2170  HOLD C : LABEL PC, "DIFFERENCE"
2190  STOP
```

6. Press Program Call button #1 on the DPO. This selects N=100, giving one hundred averages. After a moment, a 45^{o} trace should appear on the DPO screen and flicker, indicating that averaging is taking place. When averaging is completed, the display on the screen of the DPO should resemble one of those shown in Fig. 3-3.

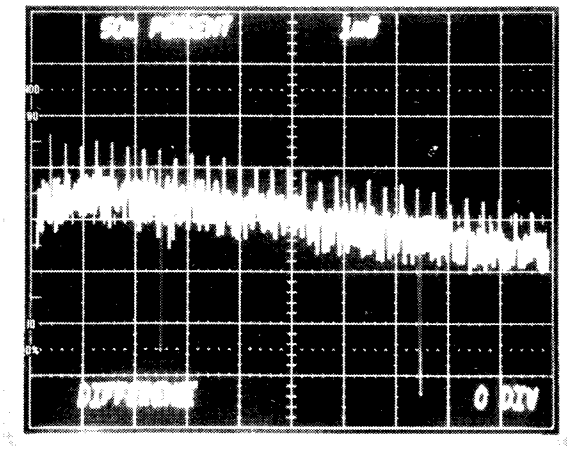
7. The display will contain noise, and may differ slightly from those in Fig. 3-3. However, any of the 32 spikes showing above or below the noise line indicates that the LSB GAIN (R75) requires adjustment.

8. Set LSB GAIN, see Fig. 3-1, a few degrees to either side of its present setting. Press Program Call button #1 and observe the display when averaging is completed. This procedure must be repeated several times until the display is essentially free of the 32 spikes above or below the noise line. More resolution can be obtained by pressing Program Call button #2 or #3 to increase the number of averages. Fig. 3-3C shows the display when LSB GAIN is properly adjusted.



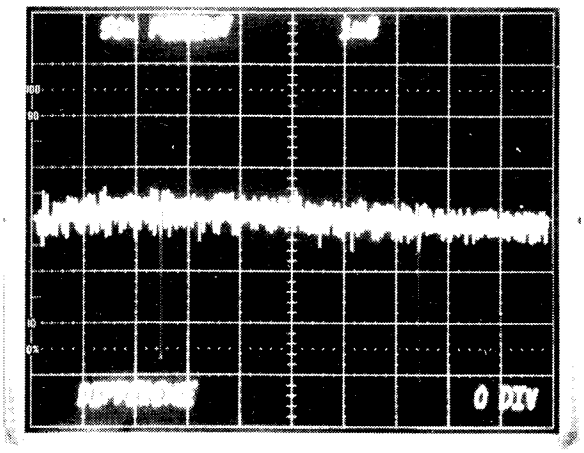
1809-11

Fig. 3-3A.
R75 Incorrect
(too far CCW).



1809-12

Fig. 3-3B.
R75 Incorrect
(too far CW).



1809-13

Fig. 3-3C.
R75 Correct
(approximately
center of range).

9. After the proper setting has been made for LSB GAIN, turn off the DPO and remove the 14-inch Tektronix coaxial cable from the A-D Converter card and the Sample-and-Hold card. Remove the Card Extender and slide the A-D Converter part-way back in. Plug in the Tektronix coaxial cable, which was left in the instrument, into J-80 and then slide the A-D Converter back fully into place. Plug the other end of the coaxial cable into J-55 on the Sample-and-Hold card. Remove J-180, on this board, and replace it one position towards the front of the DPO. Close the P7001 front panel and replace the four phillips-head screws.

NOTE

General service information may be found in the P7001 Service Manual, 070-1882-00.

@

REPLACEABLE PARTS LIST

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                - - - * - - -
   Detail Part of Assembly and/or Component
   Attaching parts for Detail Part
                - - - * - - -
      Parts of Detail Part
      Attaching parts for Parts of Detail Part
                - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
02114	FERROXCUBE CORPORATION	PO BOX 359, MARION ROAD	SAUGERTIES, NY 12477
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MURTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07910	TELEDYNE SEMICONDUCTOR	12515 CHADRON AVE.	HAWTHORNE, CA 90250
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
18677	SCANBE MFG. CORP.	3445 FLETCHER AVE.	EL MONTE, CA 91731
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E WASHINGTON STREET P O BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
	670-2379-00	B010100	B059999	CKT BOARD ASSY:A-D CONVERTER	80009	670-2379-00
	670-2379-01	B060000	B070394	CKT BOARD ASSY:A-D CONVERTER	80009	670-2379-01
	670-2379-02	B070395		CKT BOARD ASSY:A-D CONVERTER	80009	670-2379-02
C01	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020FL
C02	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020FL
C05	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C05	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C06	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C06	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C08	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
C09	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C09	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C10	290-0524-00			CAP.,FXD,ELCTLT:4.7UF,20%,10V	90201	TDC475M010EL
C12	290-0532-00			CAP.,FXD,ELCTLT:150UF,20%,6V	90201	TDC157M006WLC
C15	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C15	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C18	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C18	283-0010-00	B040000		CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C23	281-0623-00			CAP.,FXD,CER DI:650PF,5%,500V	04222	7001-1362
C26	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C26	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C29	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C29	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C31	281-0549-00	B010100	B070394	CAP.,FXD,CER DI:68PF,10%,500V	72982	301-000U2J0680K
C31	281-0550-00	B070395		CAP.,FXD,CER DI:120PF,10%,500V	04222	7001-1373
C33	281-0623-00			CAP.,FXD,CER DI:650PF,5%,500V	04222	7001-1362
C35	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C35	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C37	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C37	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C39	281-0551-00			CAP.,FXD,CER DI:390PF,10%,500V	04222	7001-1363
C40	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C41	281-0623-00			CAP.,FXD,CER DI:650PF,5%,500V	04222	7001-1362
C43	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C44	290-0523-00			CAP.,FXD,ELCTLT:2.2UF,20%,20V	56289	196D225X0020HA1
C47	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	56289	19C606
C48	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
C49	281-0580-00	B010100	B059999	CAP.,FXD,CER DI:470PF,10%,500V	04222	7001-1374
C49	283-0047-00	B060000		CAP.,FXD,CER DI:270PF,5%,500V	72982	861-518B271J
C51	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C53	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C54	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C55	281-0634-00			CAP.,FXD,CER DI:10PF,+/-0.25PF,500V	72982	374-011C0G0100C
C56	281-0523-00	B010100	B059999	CAP.,FXD,CER DI:100PF,+/-20PF,500V	72982	301-000U2M0101M
C56	281-0513-00	B060000		CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	72982	301-000P2G0270M
C57	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	56289	19C606
C58	281-0551-00			CAP.,FXD,CER DI:390PF,10%,500V	04222	7001-1363
C59	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C59	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C66	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C66	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C70	281-0093-00			CAP.,VAR,CER DI:5.5-18PF	72982	538-011A5.5-18

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C71	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
C74	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C75	281-0628-00			CAP.,FXD,CER DI:15PF,5%,500V	72982	301-000C0G0150J
C77	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C78	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C78	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C82	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C90	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C90	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C91	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C112	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C112	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C114	283-0010-00	B010100	B039999	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
C114	283-0111-00	B040000		CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C115	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
CR49	152-0141-02	XB060000		SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR62	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR63	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR72	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR73	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR80	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR81	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
J80	131-1003-00			CONNECTOR BODY,:CKT CD MT,3 PRONG	80009	131-1003-00
L70	276-0532-00			SHIELDING BEAD,:	02114	56-590-65/4A6
L71	276-0532-00			SHIELDING BEAD,:	02114	56-590-65/4A6
L74	276-0543-00			SHLD BEAD,ELEK:	80009	276-0543-00
L75	276-0543-00			SHLD BEAD,ELEK:	80009	276-0543-00
Q20	151-0190-00			TRANSISTOR:SILICON,NPN	80009	151-0190-00
Q21	151-0190-00			TRANSISTOR:SILICON,NPN	80009	151-0190-00
Q30	151-0190-00			TRANSISTOR:SILICON,NPN	80009	151-0190-00
Q31	151-0190-00			TRANSISTOR:SILICON,NPN	80009	151-0190-00
Q41	151-0302-00			TRANSISTOR:SILICON,NPN	04713	2N2222A
Q60	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	80009	151-0367-00
Q61	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	80009	151-0367-00
R01	308-0304-00			RES.,FXD,WW:1.5K OHM,1%,3W	91637	RS2B-B15000F
R02	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
R03	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
R08	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
R20	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R21	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R22	315-0161-00			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
R23	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
R24	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R25	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R30	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R31	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R32	315-0161-00			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
R33	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
R34	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R35	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R39	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R41	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R42	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R44	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R46	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R47	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R49	315-0101-00	XB060000		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R50	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R51	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
R52	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R53	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R55	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
R57	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R58	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R60	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
R61	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
R62	321-0207-00			RES.,FXD,FILM:1.4K OHM,1%,0.125W	91637	MFF1816G14000F
R63	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R64	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
R65	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R70	321-0126-00			RES.,FXD,FILM:200 OHM,1%,0.125W	91637	MFF1816G200R0F
R71	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R73	321-0155-00			RES.,FXD,FILM:402 OHM,1%,0.125W	91637	MFF1816G402R0F
R74	321-0093-00			RES.,FXD,FILM:90.9 OHM,1%,0.125W	91637	MFF1816G90R90F
R75	311-1007-00			RES.,VAR,NONWIR:20 OHM,20%,0.50W	73138	82-38-0
R77	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
R79	321-0001-00			RES.,FXD,FILM:10 OHM,1%,0.125W	75042	CEAT0-10R00F
R80	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
R90	308-0662-00			RES.,FXD,WW:64 OHM,0.08%,0.125W	91637	WWP225-A64001X
R91	308-0661-00			RES.,FXD,WW:32KOHM,0.04%,0.125W	91637	WWP225-A32001X
R92	308-0660-00			RES.,FXD,WW:16K OHM,0.2%,0.125W	91637	WWP225-H16001M
R93	308-0659-00			RES.,FXD,WW:8K OHM,0.01%,0.125W	91637	WWP225-800000L
R94	308-0658-00			RES.,FXD,WW:4K OHM,0.01%,0.125W	91637	WWP225-A40000L
R95	321-0165-00			RES.,FXD,FILM:511 OHM,1%,0.125W	91637	MFF1816G511R0F
R99	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R100	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R108	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R110	308-0662-00			RES.,FXD,WW:64K OHM,0.08%,0.125W	91637	WWP225-A64001X
R111	308-0661-00			RES.,FXD,WW:32K OHM,0.04%,0.125W	91637	WWP225-A32001X
R112	308-0660-00			RES.,FXD,WW:16K OHM,0.2%,0.125W	91637	WWP225-H16001M
R113	308-0659-00			RES.,FXD,WW:8K OHM,0.01%,0.125W	91637	WWP225-A80000L
R114	308-0658-00			RES.,FXD,WW:4K OHM,0.01%,0.125W	91637	WWP225-A40000L
R115	321-0165-00			RES.,FXD,FILM:511 OHM,1%,0.125W	91637	MFF1816G511R0F
U01	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U02	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U03	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U04	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U05	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U11	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U12	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U13	156-0150-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7437N
U14	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	01295	SN74174N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U15	156-0145-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	01295	SN7438N
U21	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U22	156-0075-00			MICROCIRCUIT,DI:SGL 8-BIT DATA SEL MUX	80009	156-0075-00
U23	156-0165-00			MICROCIRCUIT,DI:DUAL 4-INPUT POS NOR GATE	01295	SN7425N
U24	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U25	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U31	156-0120-00			MICROCIRCUIT,DI:SINGLE 4-BIT R/L SHIFT REG	01295	SN7495AN
U32	156-0129-00			MICROCIRCUIT,DI:QUAD 2-INPUT GATE	01295	SN7408N
U33	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U34	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U35	156-0047-00			MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U41	156-0075-00			MICROCIRCUIT,DI:SGL 8-BIT DATA SEL MUX	80009	156-0075-00
U42	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U43	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U44	156-0072-00			MICROCIRCUIT,DI:MONOSTABLE MV,TTL	27014	DM74121N
U45	156-0047-00			MICROCIRCUIT,DI:TPL 3-INPUT POS NAND GATE	80009	156-0047-00
U52	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U53	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U54	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN7404N
U55	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U61	156-0251-00			MICROCIRCUIT,DI:VOLTAGE COMPENSATOR	18324	E5059K/NE529K
U62	156-0249-00			MICROCIRCUIT,DI:10 BIT INV BUFFER REG	80009	156-0249-00
U64	156-0249-00			MICROCIRCUIT,DI:10 BIT INV BUFFER REG	80009	156-0249-00
U70	155-0035-00			MICROCIRCUIT,LI:QUAD OPERATIONAL AMPL	80009	155-0035-00
U72	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U74	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U75	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U82	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U84	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U85	156-0117-00			MICROCIRCUIT,DI:SYNC 4-BIT BINARY COUNTER	01295	SN74161N
U90	155-0038-02			MICROCIRCUIT,DI:D-A CONVERTER	80009	155-0038-02
U92	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U94	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U95	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U102	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U104	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U105	156-0041-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	27014	DM7474N
U110	155-0038-02			MICROCIRCUIT,DI:D-A CONVERTER	80009	155-0038-02
U112	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U114	156-0037-00			MICROCIRCUIT,DI:2-INPUT +AND/OR/INVERT GATE	80009	156-0037-00
U115	156-0131-00			MICROCIRCUIT,DI:8-BIT SER TO PARALLEL SHF	80009	156-0131-00
VR61	152-0278-00			SEMICOND DEVICE:ZENER,0.4W,3V,5%	07910	1N4372A

MECHANICAL PARTS LIST

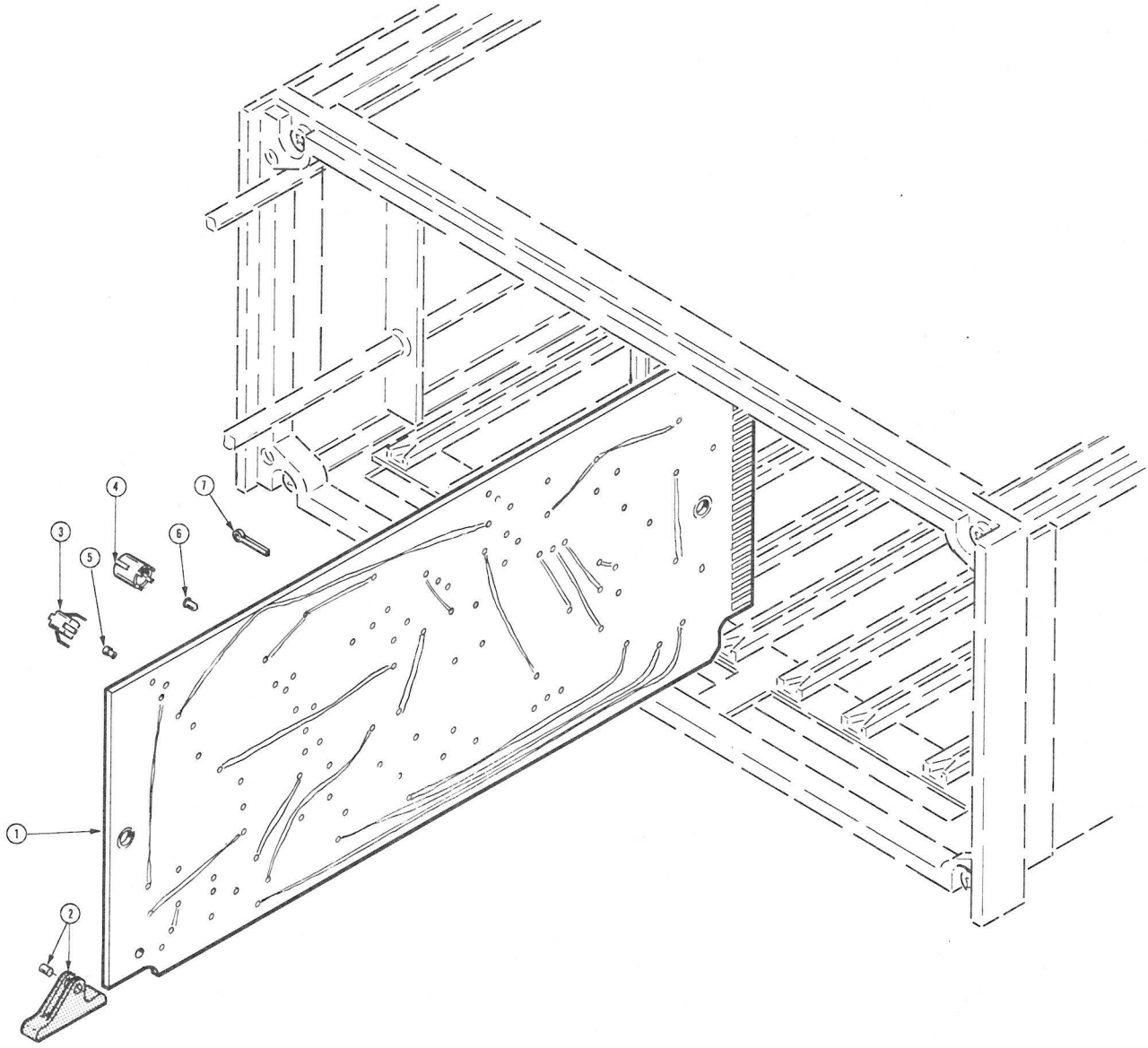
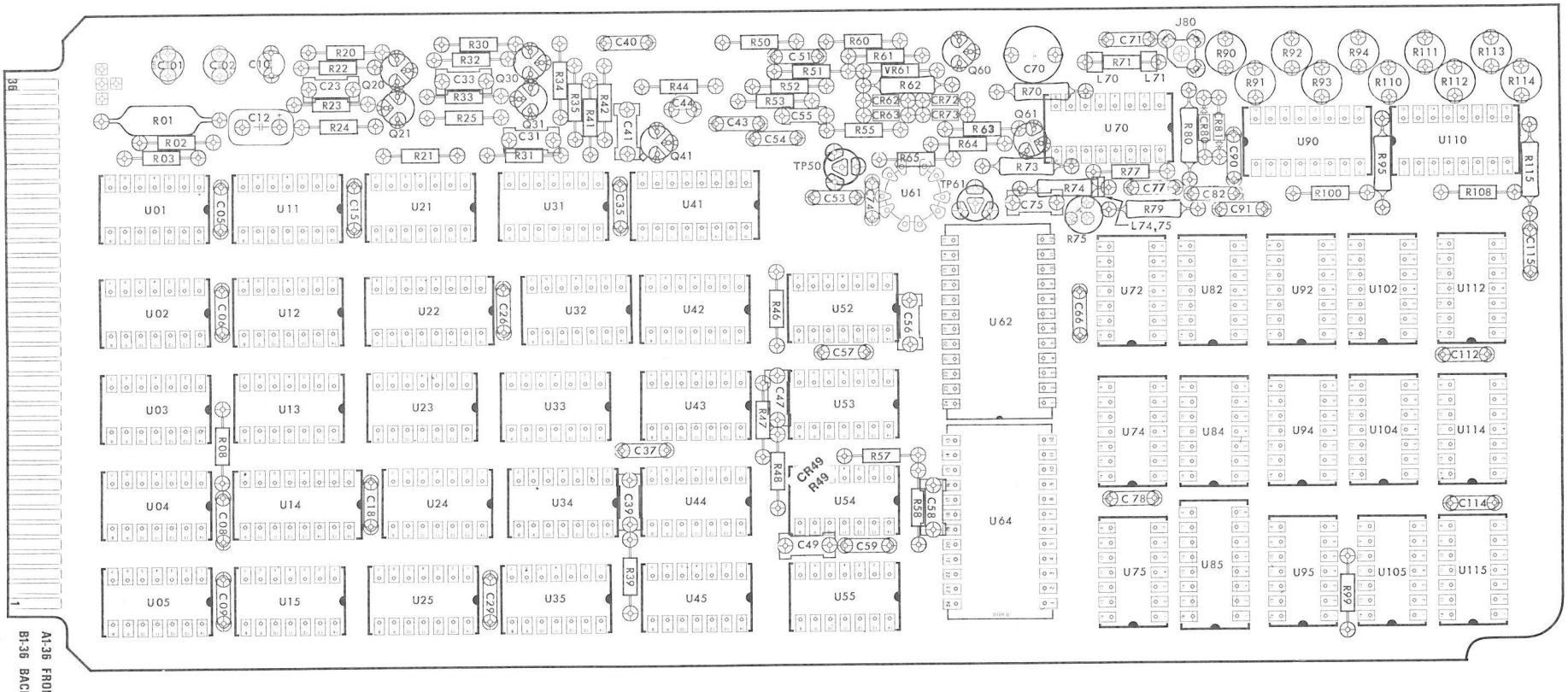


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			1		CKT BOARD ASSY:A/D CONVERTER(SEE EPL)		
-2	105-0144-00			1		EJECTOR,CKT CD:MOLD PLASTIC,W/ROLL PIN	18677	S203
-3	131-1003-00			1		CONNECTOR BODY,:CKT CD MT,3 PRONG	80009	131-1003-00
-4	131-1436-00			2		RCPT,COAX CABLE:	80009	131-1436-00
-5	136-0252-04			125		SOCKET,PIN TERM:0.188 INCH LONG	22526	75060
-6	136-0333-00			2		SOCKET,PIN TERM:0.138 INCH LONG	00779	1-331677-4
-7	214-0579-00			3		TERM.,TEST PT:0.40 INCH LONG	80009	214-0579-00
						STANDARD ACCESSORIES		
	070-1809-00			1		MANUAL,TECH:	80009	070-1809-00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A1-36 FRONT
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J80
C01
C02
C10
R20
R22
C23
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Q20
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R114
R115
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C59
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C39
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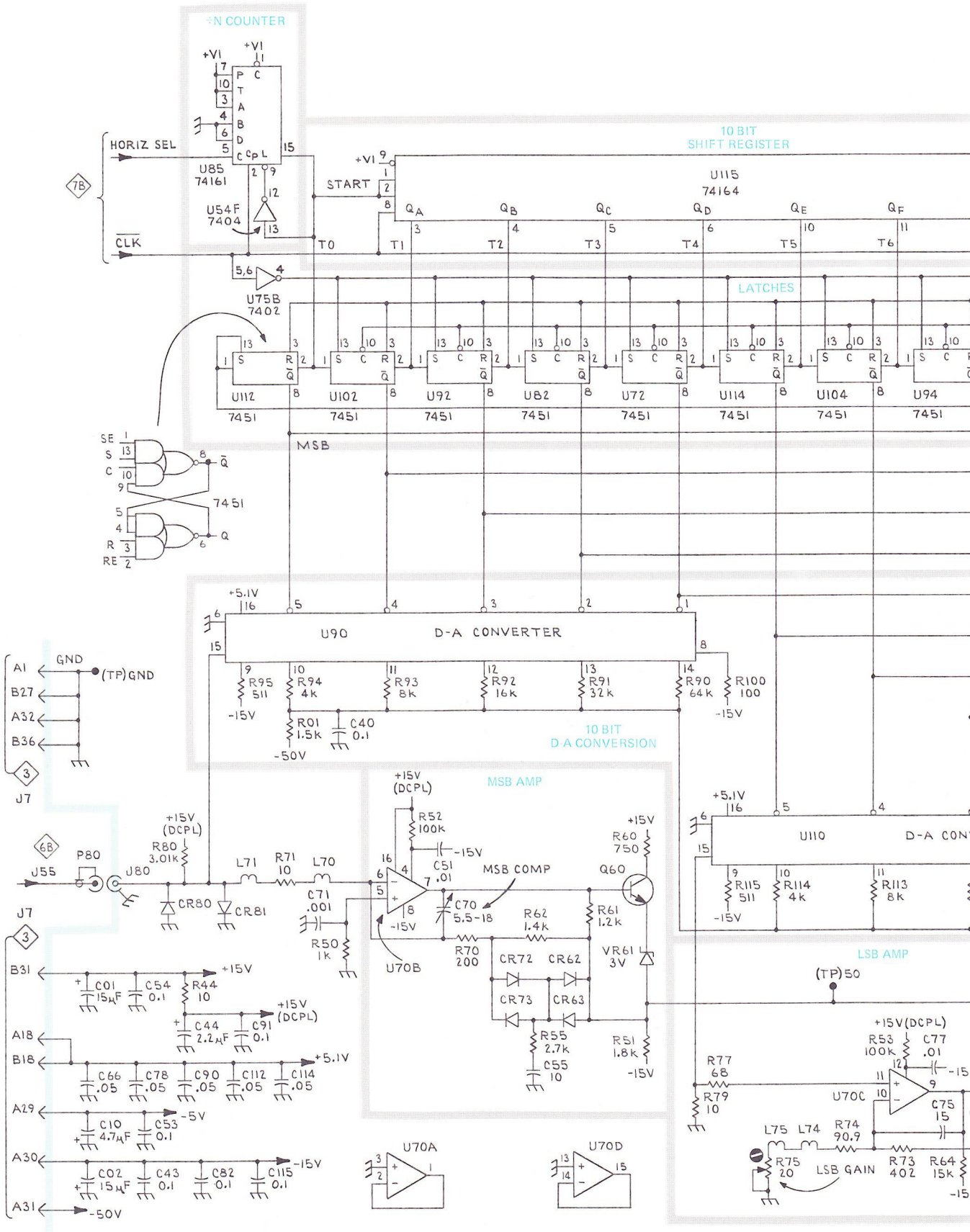
U105
U115



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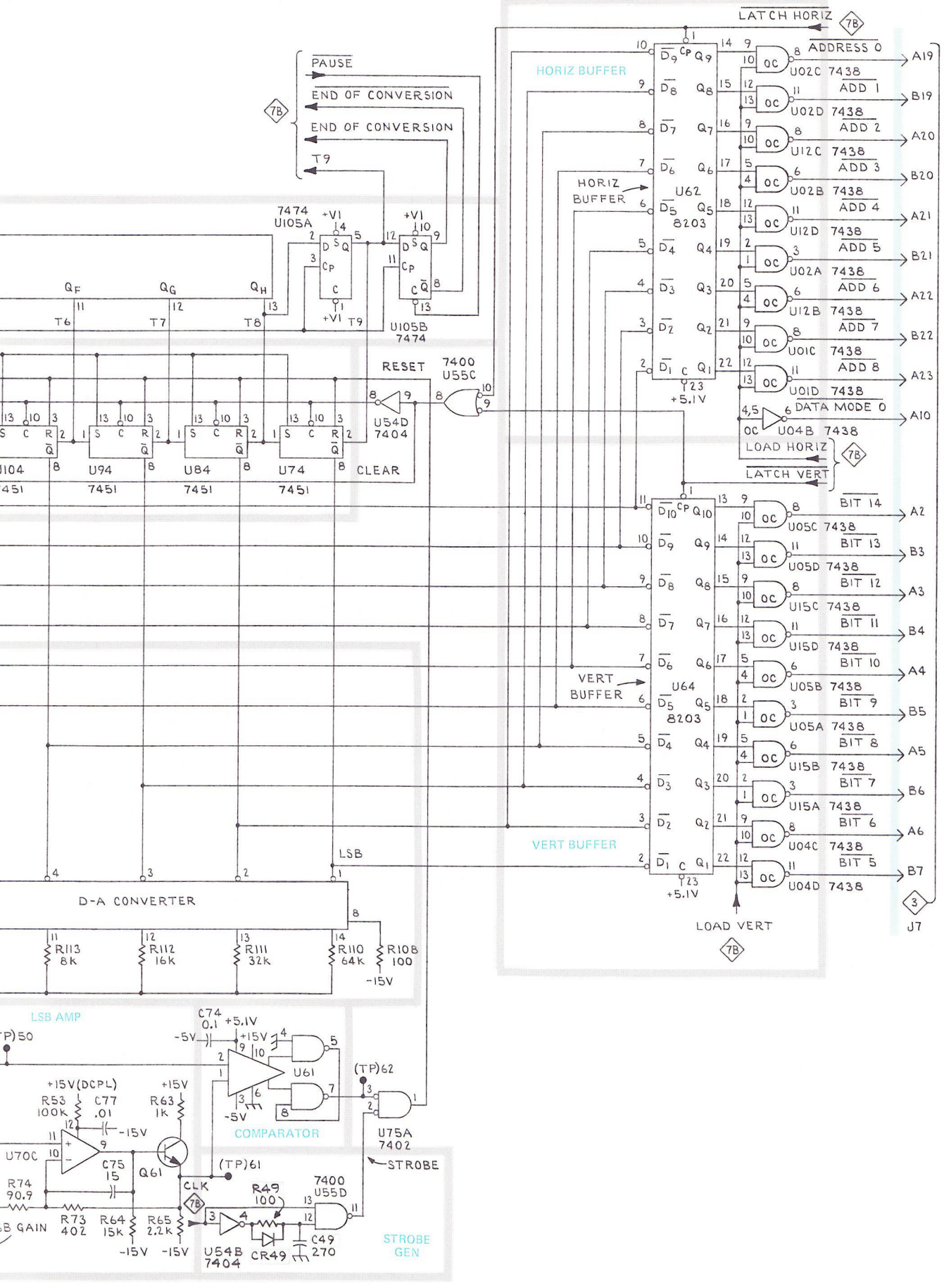
1809-14
REV. A, JAN. 1978



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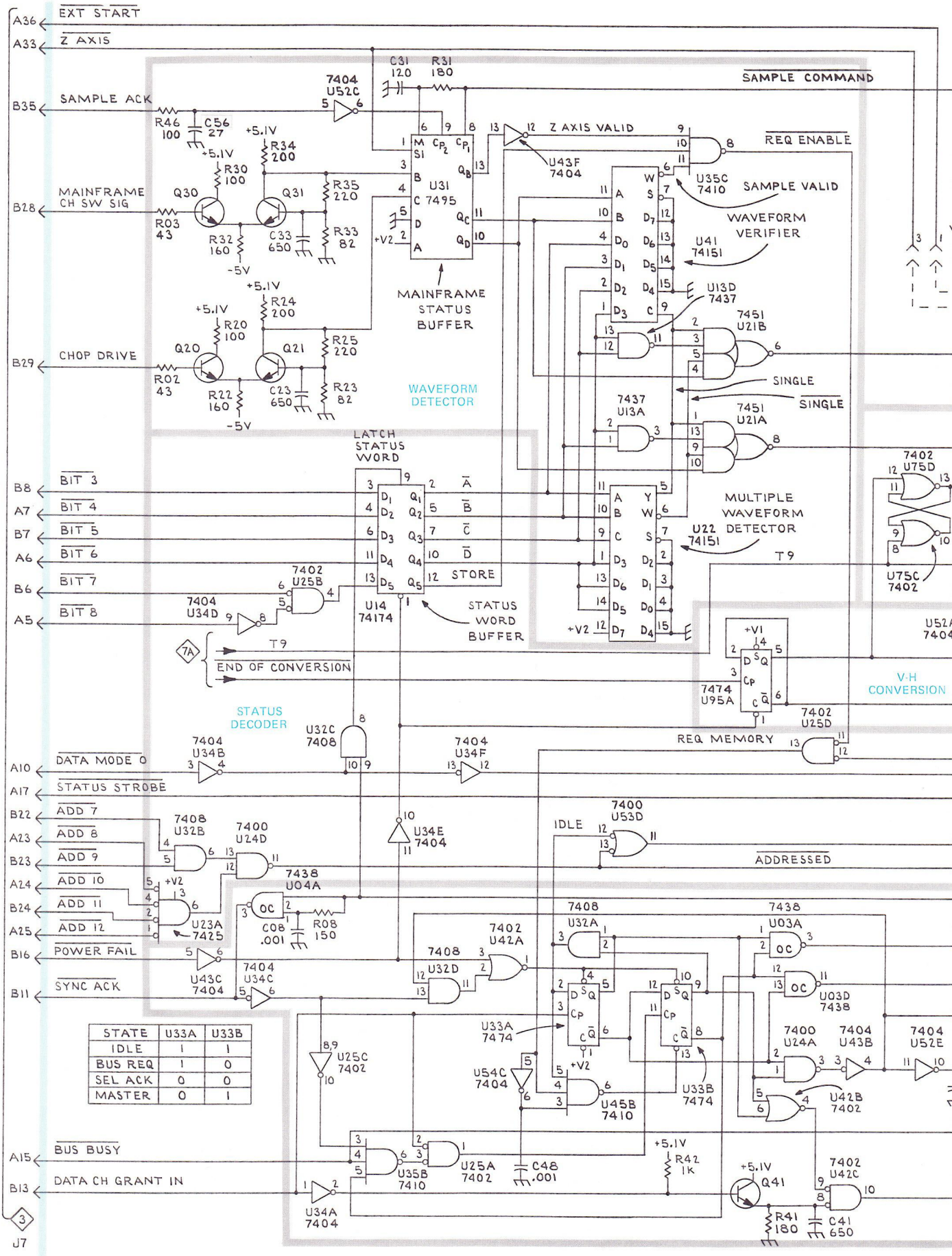
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SAMPLE ACK
MAINFRAME CH SW SIG
CHOP DRIVE
MAINFRAME STATUS BUFFER
WAVEFORM DETECTOR
Z AXIS VALID
REQ ENABLE
SAMPLE VALID
WAVEFORM VERIFIER
SINGLE
MULTIPLE WAVEFORM DETECTOR
LATCH STATUS WORD
STATUS WORD BUFFER
STORE
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
T9
END OF CONVERSION
V-H CONVERSION
STATUS DECODER
REQ MEMORY
DATA MODE 0
STATUS STROBE
ADD 7
ADD 8
ADD 9
ADD 10
ADD 11
ADD 12
IDLE
ADDRESSED
POWER FAIL
SYNC ACK
BUS BUSY
DATA CH GRANT IN
U31 7495
U35C 7410
U41 74151
U13D 7437
U21B 7451
U13A 7437
U21A 7451
U22 74151
U14 74174
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Q41
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+V1
+V2
-5V
R46 100
C56 27
R30 100
R34 200
R35 220
R32 160
C33 650
R33 82
R03 43
R20 100
R24 200
R25 220
R22 160
C23 650
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C08 .001
R08 150
C48 .001
R42 1K
R41 180
C41 650
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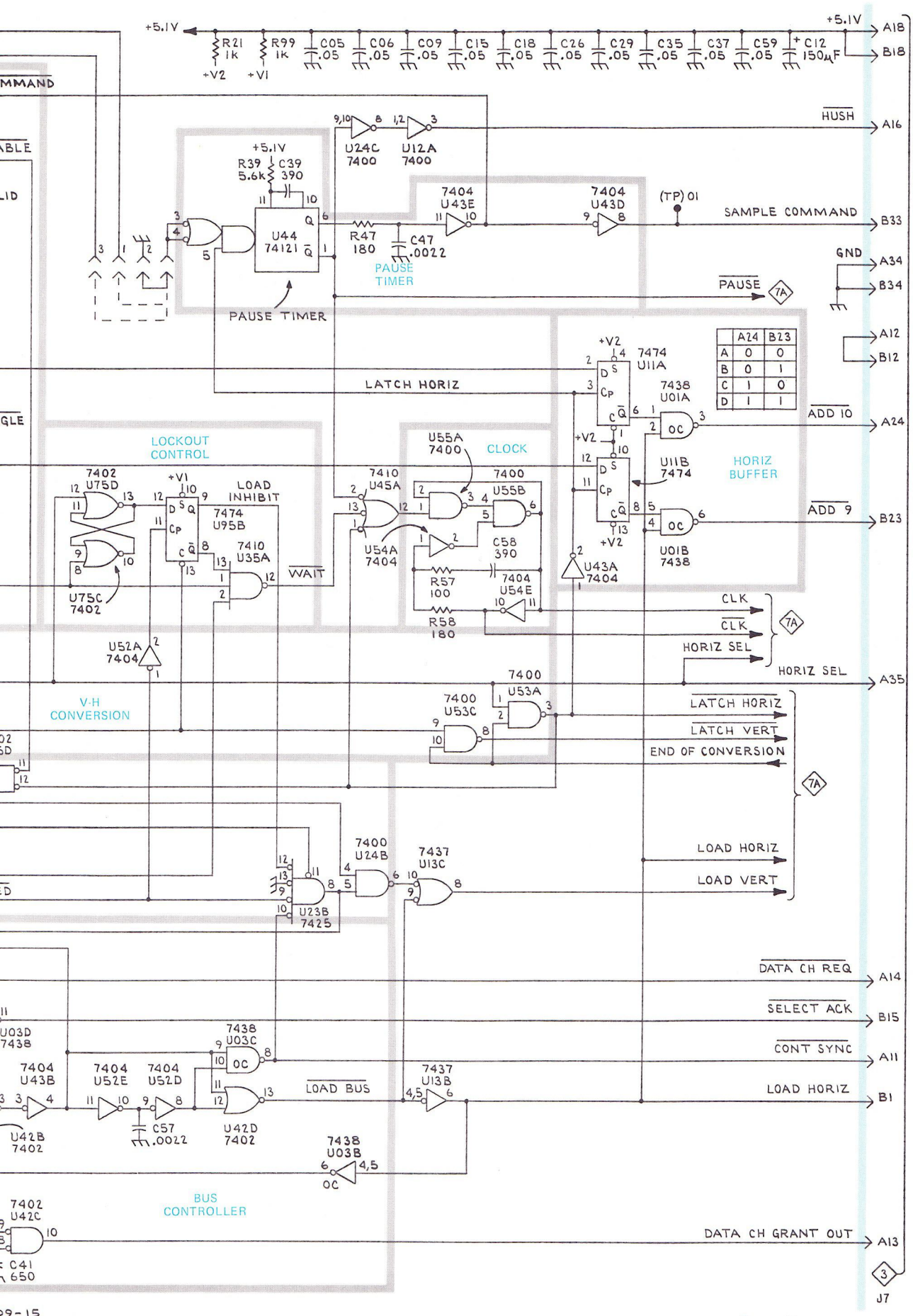
SEL ACK | 0 | 0
MASTER | 0 | 1
P7001
1809-15
REV A, JAN. 1978



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B	0	1
C	1	0
D	1	1

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Change Reference: M34035 Date: 6-6-79

Product: P7001 A-D CONVERTER 070-1809-00 EFF SN B100681

CHANGE	DESCRIPTION

ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

Q20	151-0190-07	TRANSISTOR:SILICON,NPN
Q21	151-0190-07	TRANSISTOR:SILICON,NPN
Q30	151-0190-07	TRANSISTOR:SILICON,NPN
Q31	151-0190-07	TRANSISTOR:SILICON,NPN
U01	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U02	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U03	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U04	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U05	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U11	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U12	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U15	156-0145-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR
U24	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U33	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U53	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U55	156-0030-02	MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE
U95	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP
U105	156-0041-05	MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP